

What is claimed is:

- 1 1. A method of manufacturing an integrated circuit package, comprising:
2 installing a carrier onto an upper surface of a substrate, wherein said
3 carrier defines a cavity;
4 attaching a semiconductor die to said upper surface of said substrate
5 within said cavity of said carrier;
6 aligning an assembly over said semiconductor die, wherein said assembly
7 comprises a heat sink and a thermally conductive element;
8 resting said assembly on said carrier such that said thermally conductive
9 element does not directly contact said semiconductor die; and
10 encapsulating said cavity to form a prepackage such that a portion of said
11 heat sink is exposed to the surroundings of said package.
- 1 2. The method of claim 1, wherein said assembly is rested on said carrier
2 such that said thermally conductive element and said semiconductor die are separated by
3 a distance of about five (5) mils or less.
- 1 3. The method of claim 1, wherein said attaching said semiconductor die to
2 said upper surface of said substrate is by a direct chip attachment.
- 1 4. The method of claim 1, further comprising singulating said prepackage to
2 form said package, wherein a top portion and a side portion of said heat sink are exposed
3 to the surroundings of said package.
- 1 5. A method of manufacturing an integrated circuit package, comprising:
2 installing a carrier onto a substrate;

3 attaching a semiconductor die to said substrate;
4 aligning an assembly over said semiconductor die, wherein said assembly
5 comprises a heat sink and a thermally conductive element;
6 resting said assembly on said carrier such that said thermally conductive
7 element does not directly contact said semiconductor die; and
8 encapsulating said thermally conductive element and said heat sink such
9 that a portion of said heat sink is exposed to the surroundings of said package.